THE INVENTION CLAIMED IS:

1. A method for manufacturing an integrated circuit structure, comprising:

providing a semiconductor substrate;

forming a horizontal semiconductor fin on top of the semiconductor substrate;

forming an access transistor gate on top of the semiconductor substrate and in contact with the horizontal semiconductor fin;

forming a thyristor gate on top of the semiconductor substrate and in contact with the horizontal semiconductor fin;

forming an access transistor from at least a portion of the horizontal semiconductor fin and the access transistor gate; and

forming a thyristor from at least a portion of the horizontal semiconductor fin and the thyristor gate, such that the access transistor is in contact with the thyristor.

2. The method of claim 1 wherein providing a semiconductor substrate and forming a horizontal semiconductor fin further comprise providing a silicon-on-insulator wafer and forming the horizontal semiconductor fin from the top silicon layer of the silicon-on-insulator wafer.

3. The method of claim 1 wherein both the access transistor gate and the thyristor gate are formed around at least a portion of the horizontal semiconductor fin.

4. The method of claim 1 further comprising forming a liner and a spacer around at least portions of the horizontal semiconductor fin, the access transistor gate, and the thyristor gate.

5. The method of claim 1 further comprising:

depositing an interlayer dielectric layer over at least the access transistor and the thyristor; and

forming at least one electrical contact through the interlayer dielectric layer to the access transistor and at least one electrical contact through the interlayer dielectric layer to the thyristor.

6. A method for manufacturing an integrated circuit structure, comprising:

providing a silicon-on-insulator semiconductor wafer;

etching a horizontal semiconductor fin from the top silicon layer of the silicon-on-insulator semiconductor wafer;

forming an access transistor gate on top of the semiconductor wafer and around and in contact with the horizontal semiconductor fin;

forming a thyristor gate on top of the semiconductor wafer and around and in contact with the horizontal semiconductor fin;

forming an access transistor from at least a portion of the horizontal semiconductor fin and the access transistor gate; and

forming a thyristor from at least a portion of the horizontal semiconductor fin and the thyristor gate, such that the access transistor is in contact with the thyristor.

7. The method of claim 6 further comprising implanting an N- lightly doped drain implantation into at least a portion of the horizontal semiconductor fin and implanting an N+ implantation into at least a portion of the horizontal semiconductor fin.

8. The method of claim 6 wherein forming the thyristor further comprises implanting at least a portion of the horizontal semiconductor fin with a deep N- implantation, followed by implanting at least a portion of the horizontal semiconductor fin with a P+ implantation.

9. The method of claim 6 further comprising forming a liner and a spacer around at least portions of the horizontal semiconductor fin, the access transistor gate, and the thyristor gate.

10. The method of claim 6 further comprising:

depositing an interlayer dielectric layer over at least the access transistor and the thyristor; and

forming at least one electrical contact through the interlayer dielectric layer to the access transistor and at least one electrical contact through the interlayer dielectric layer to the thyristor.

11. An integrated circuit structure, comprising:

a semiconductor substrate;

a horizontal semiconductor fin on top of the semiconductor substrate;

an access transistor gate on top of the semiconductor substrate and in contact with the horizontal semiconductor fin;

a thyristor gate on top of the semiconductor substrate and in contact with the horizontal semiconductor fin;

an access transistor formed from at least a portion of the horizontal semiconductor fin and the access transistor gate; and

a thyristor formed from at least a portion of the horizontal semiconductor fin and the thyristor gate, the access transistor being in contact with the thyristor.

12. The structure of claim 11 wherein the semiconductor substrate and the horizontal semiconductor fin further comprise a silicon-on-insulator wafer in which the horizontal semiconductor fin is formed from the top silicon layer of the silicon-on-insulator wafer.

13. The structure of claim 11 wherein both the access transistor gate and the thyristor gate are formed around at least a portion of the horizontal semiconductor fin.

14. The structure of claim 11 further comprising a liner and a spacer formed around at least portions of the horizontal semiconductor fin, the access transistor gate, and the thyristor gate.

15. The structure of claim 11 further comprising:

an interlayer dielectric layer over at least the access transistor and the thyristor; and

at least one electrical contact through the interlayer dielectric layer to the access transistor and at least one electrical contact through the interlayer dielectric layer to the thyristor.

16. An integrated circuit structure, comprising:

a silicon-on-insulator semiconductor wafer;

a horizontal semiconductor fin etched from the top silicon layer of the silicon-on-insulator semiconductor wafer;

an access transistor gate on top of the semiconductor wafer and formed around and in contact with the horizontal semiconductor fin;

a thyristor gate on top of the semiconductor wafer and formed around and in contact with the horizontal semiconductor fin;

an access transistor formed from at least a portion of the horizontal semiconductor fin and the access transistor gate; and

a thyristor formed from at least a portion of the horizontal semiconductor fin and the thyristor gate, such that the access transistor is in contact with the thyristor.

17. The structure of claim 16 further comprising an N- lightly doped drain implantation implanted into at least a portion of the horizontal semiconductor fin and an N+ implantation implanted into at least a portion of the horizontal semiconductor fin.

18. The structure of claim 16 wherein the thyristor further comprises a deep N- implantation implanted into at least a portion of the horizontal semiconductor fin, followed by a P+ implantation implanted into at least a portion of the horizontal semiconductor fin.

19. The structure of claim 16 further comprising a liner and a spacer formed around at least portions of the horizontal semiconductor fin, the access transistor gate, and the thyristor gate.

20. The structure of claim 16 further comprising:

an interlayer dielectric layer over at least the access transistor and the thyristor; and

at least one electrical contact through the interlayer dielectric layer to the access transistor and at least one electrical contact through the interlayer dielectric layer to the thyristor.